FIG. 1

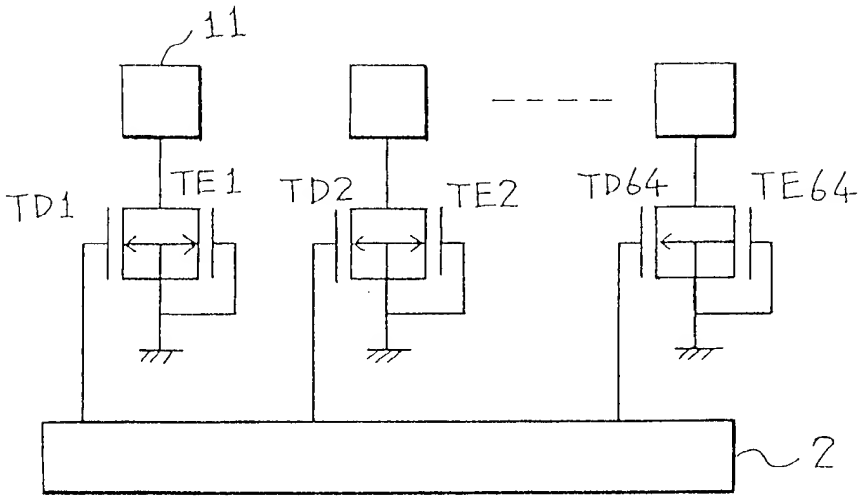


FIG. 2
PRIOR ART

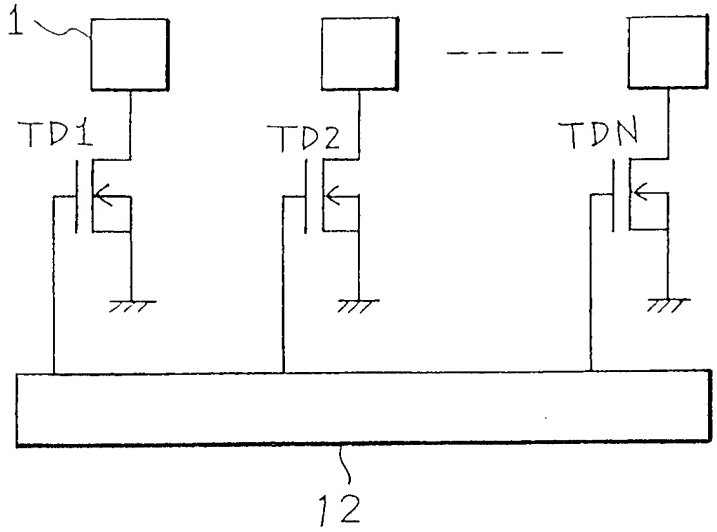


FIG. 3
PRIOR ART

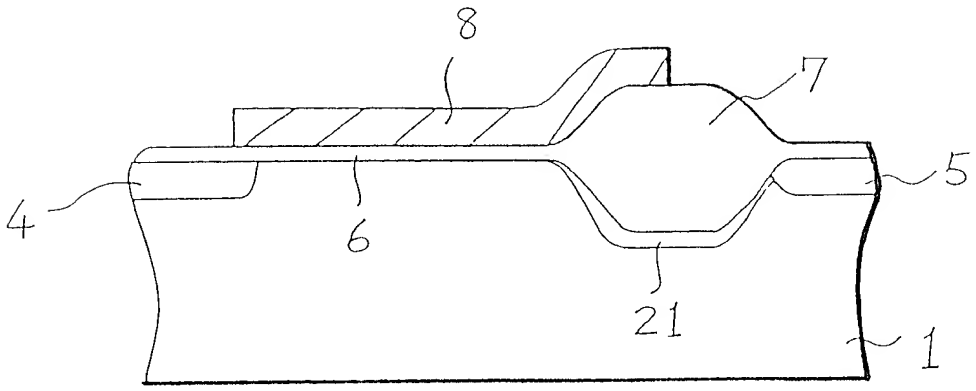


FIG. 4
PRIOR ART

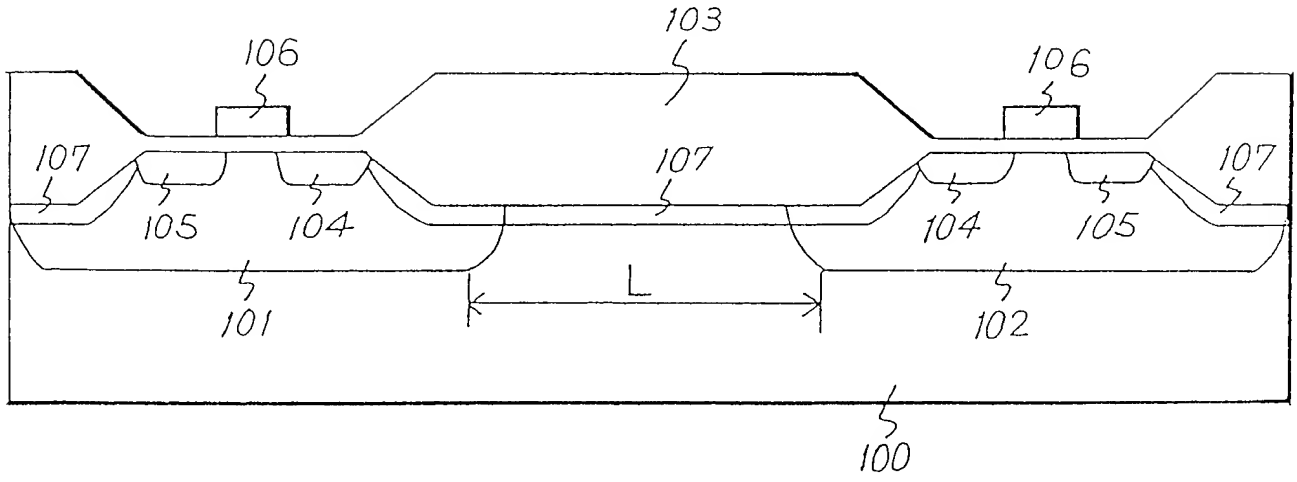


FIG. 5

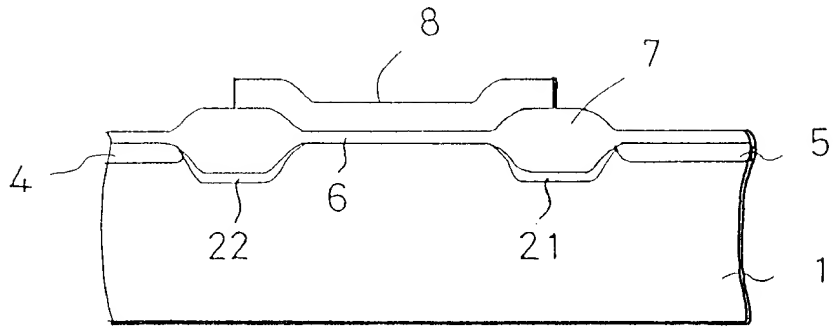


FIG. 6

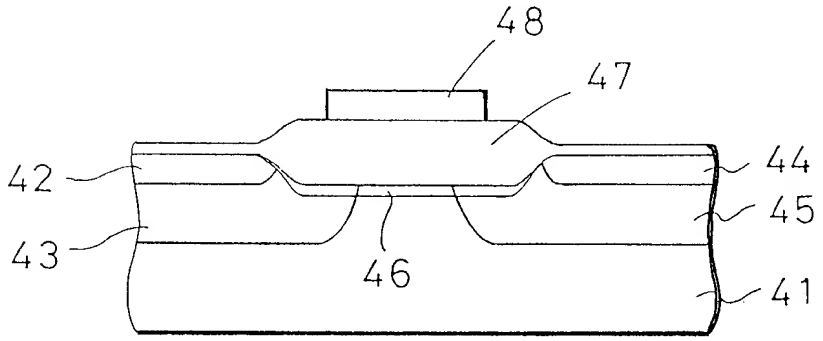


FIG. 7

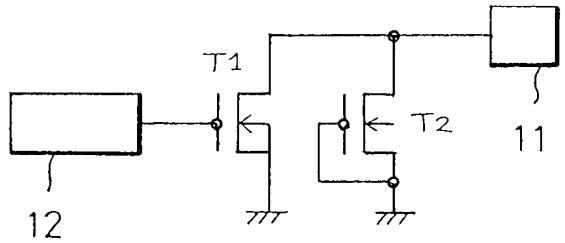


FIG. 8

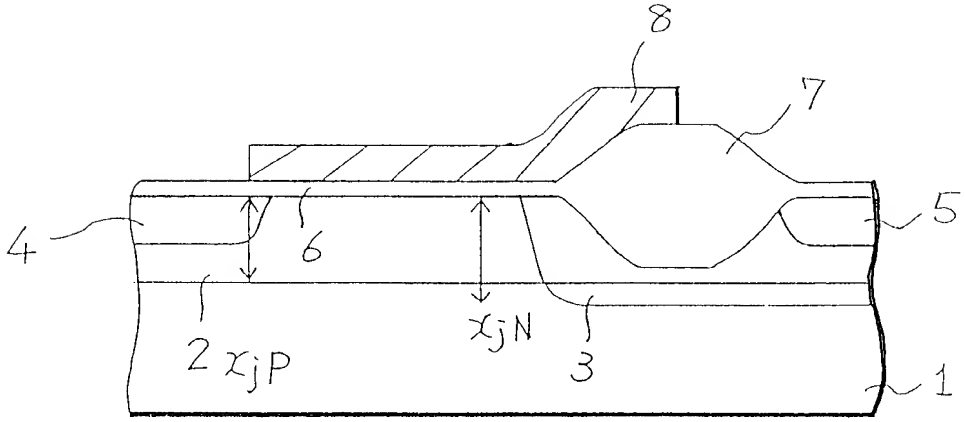


FIG. 9

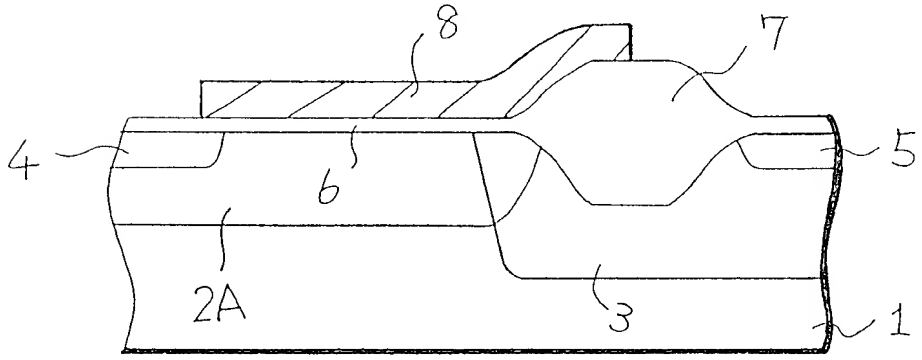


FIG. 10

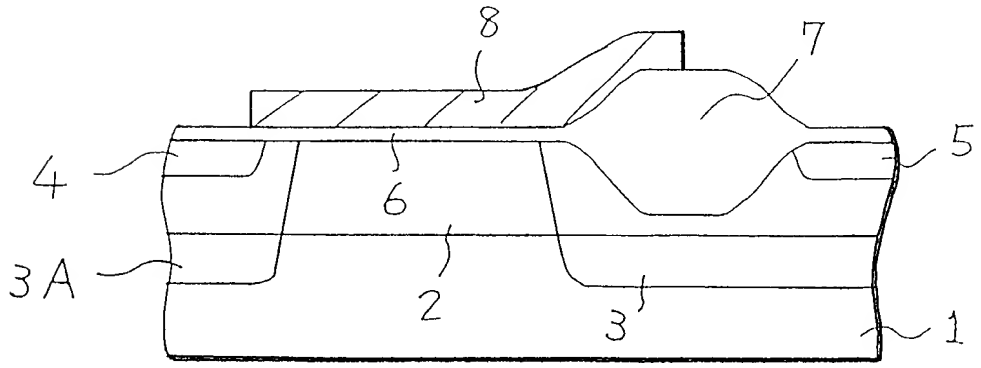


FIG. 11

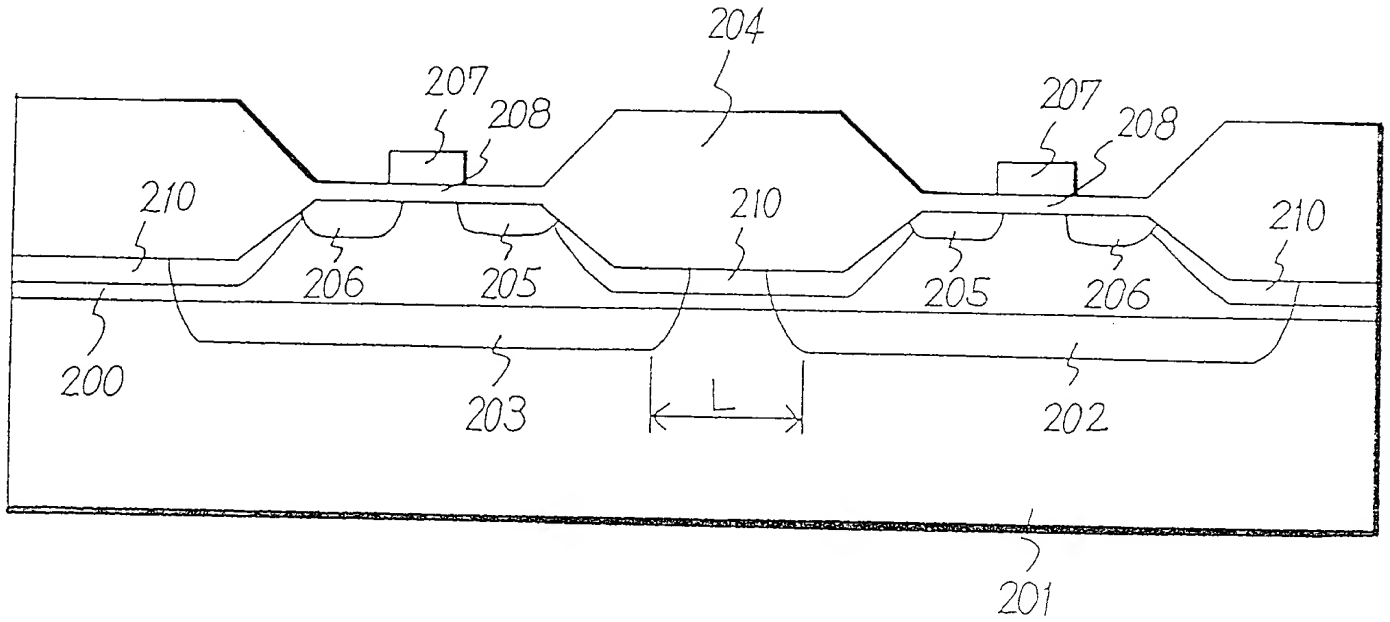


FIG. 12

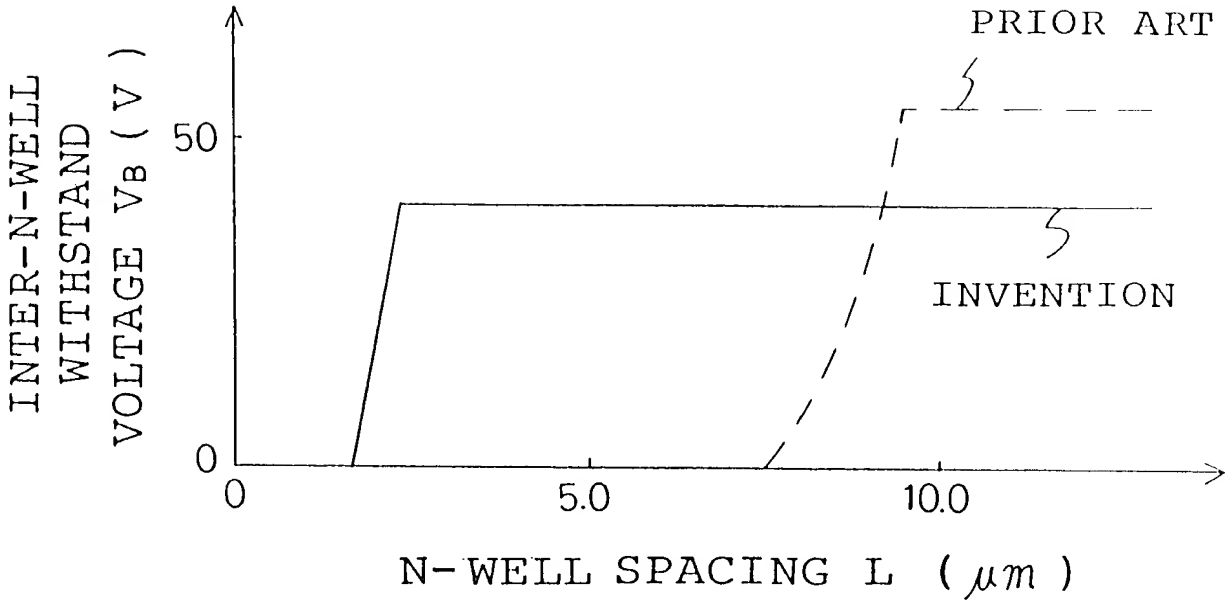

PRIOR ART
INVENTION
INTER-N-WELL WITHSTAND VOLTAGE V_B (V)
50
0
0
5.0
10.0
N-WELL SPACING L (μm)

FIG. 13

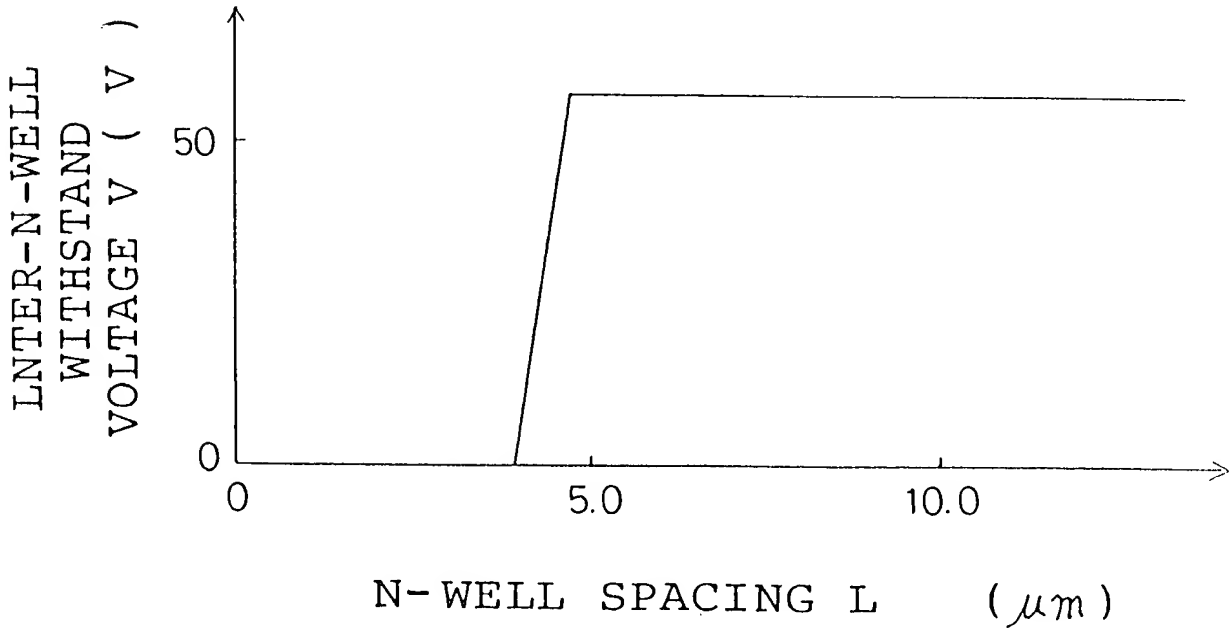

LNTER-N-WELL WITHSTAND VOLTAGE V (V)
50
0
0
5.0
10.0
N-WELL SPACING L (μm)

FIG. 14

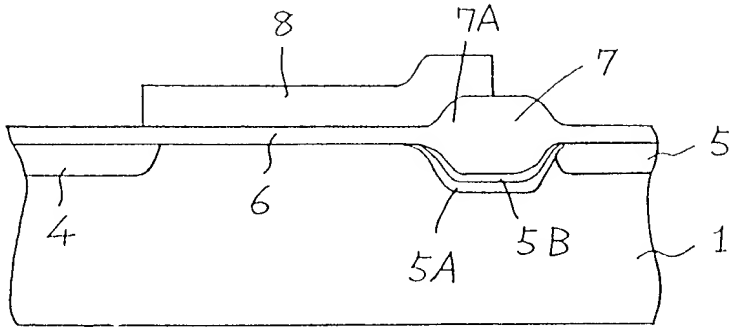

8
7A
7
5
6
4
5A
5B
1

FIG. 15

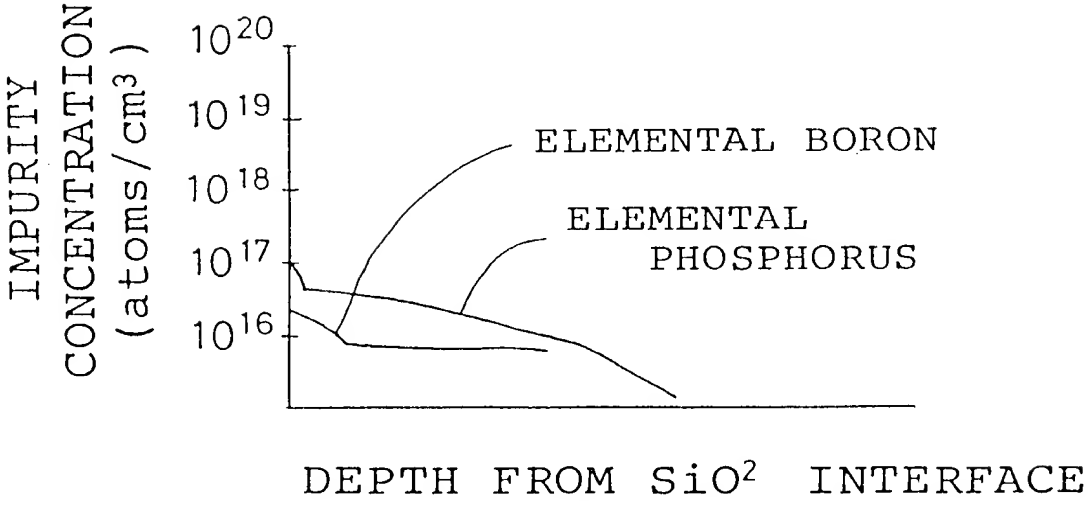

IMPURITY CONCENTRATION (atoms/cm³)
10²⁰
10¹⁹
10¹⁸
10¹⁷
10¹⁶
ELEMENTAL BORON
ELEMENTAL PHOSPHORUS
DEPTH FROM SiO² INTERFACE

FIG. 16A

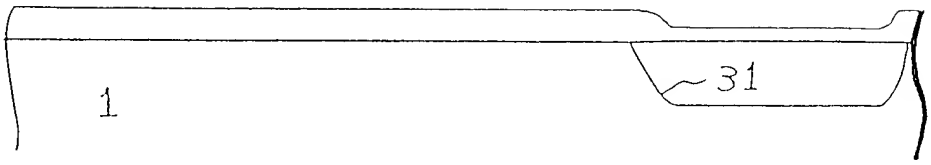


FIG. 16B

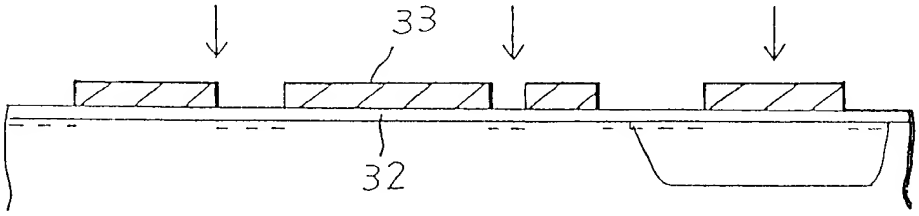


FIG. 16C

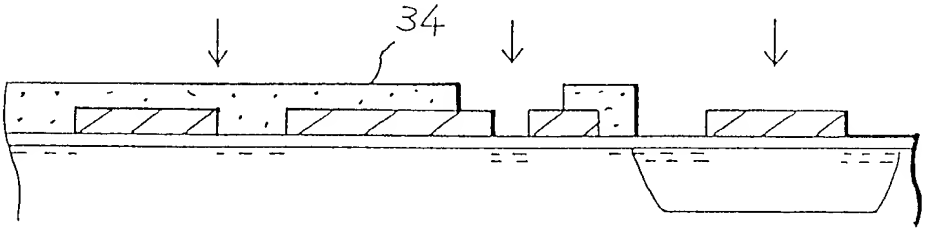


FIG. 16D

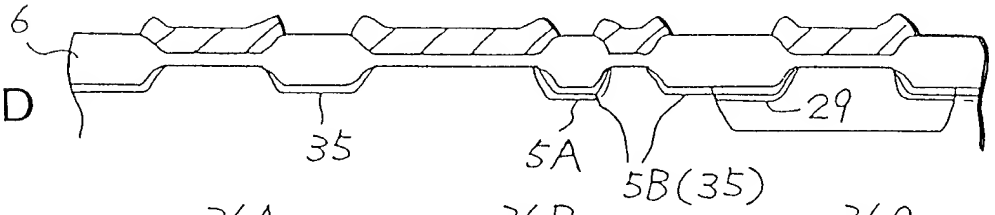
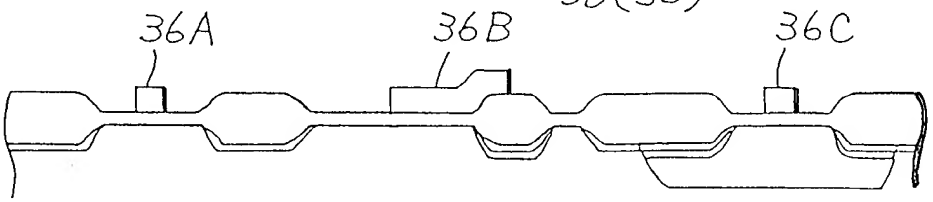


FIG. 16E



LVNMOS－TRANSISTOR　HVNMOS－TRANSISTOR　PMOS－TRANSISTOR

FIG. 16F

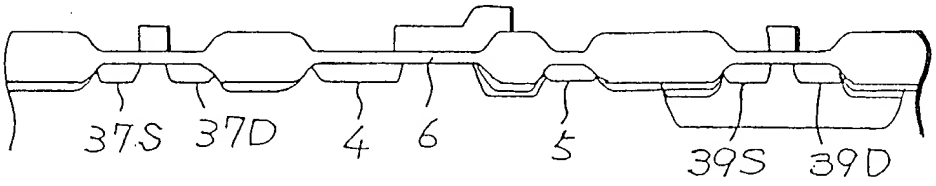


FIG. 17

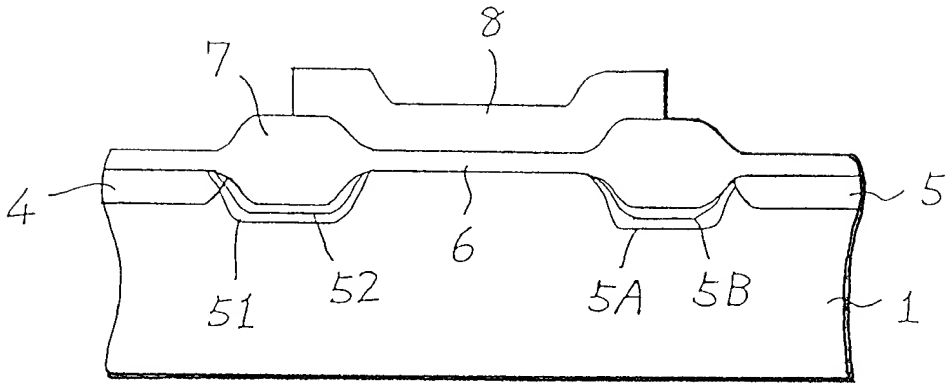


FIG. 18

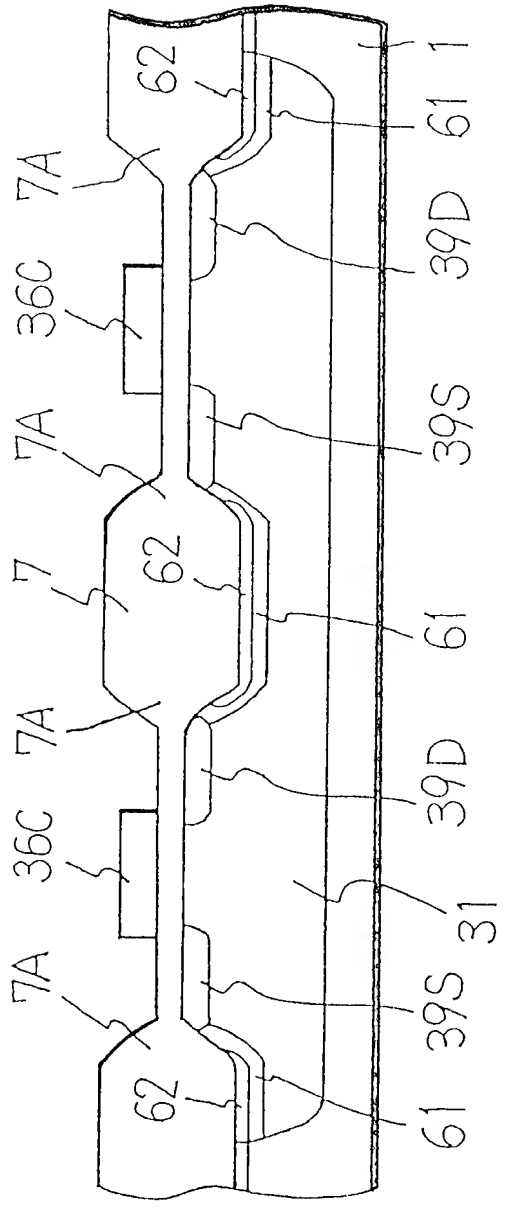


FIG. 19

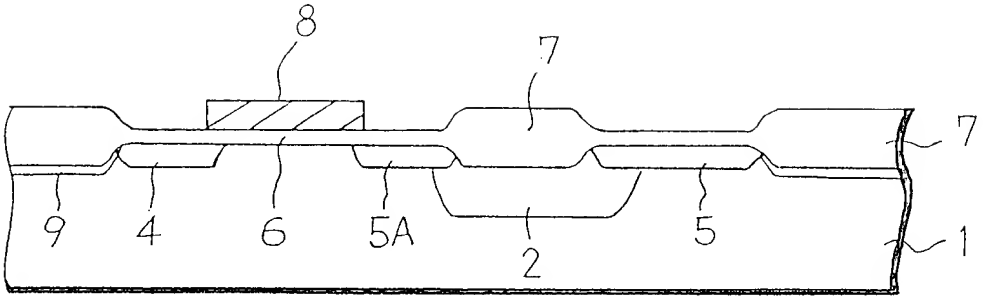


FIG. 20

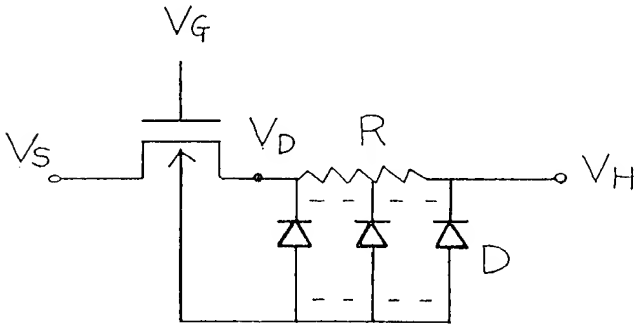


FIG. 21

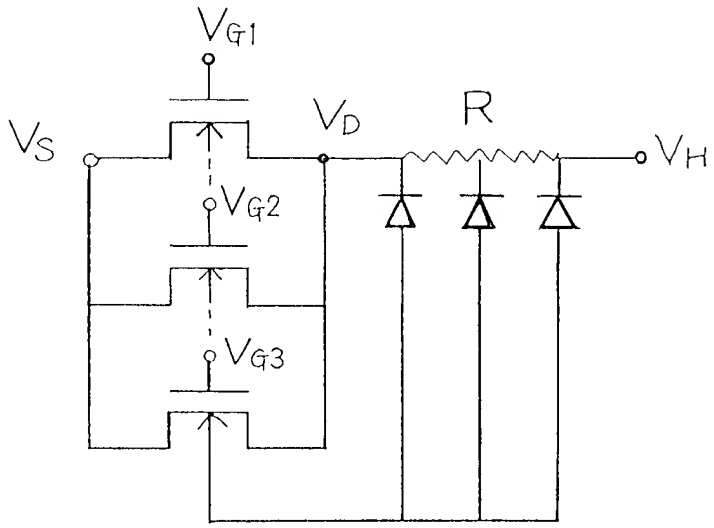


FIG. 22

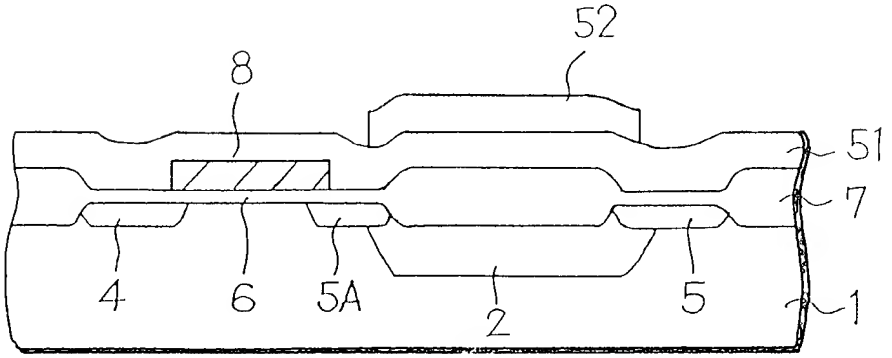


FIG. 23

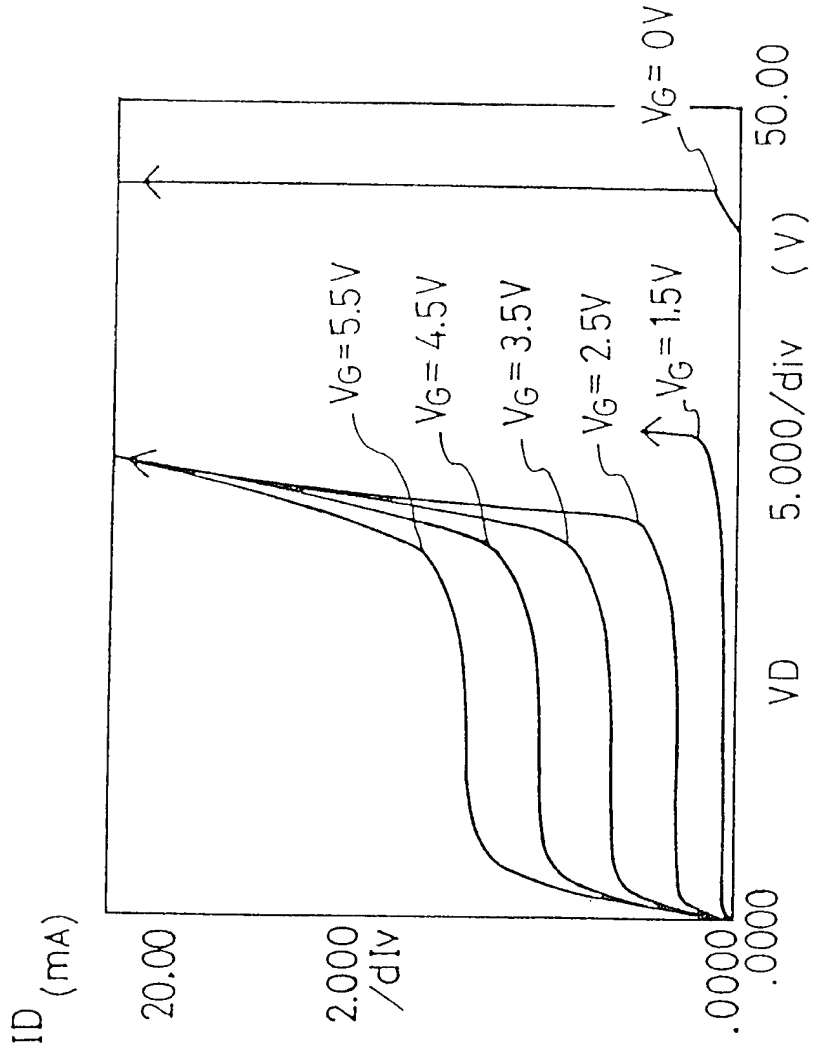

ID (mA)
20.00
2.000 /div
.0000
.0000
VD
5.000/div (V)
50.00
VG= 5.5V
VG= 4.5V
VG= 3.5V
VG= 2.5V
VG= 1.5V
VG= 0V

FIG. 24

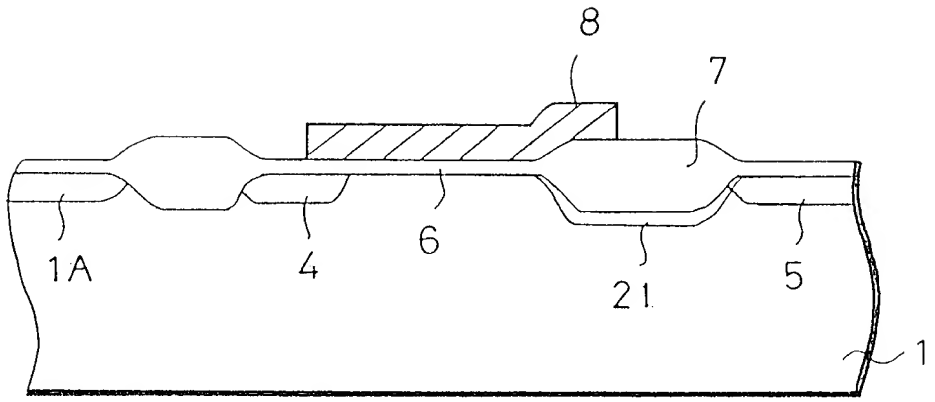


FIG. 25

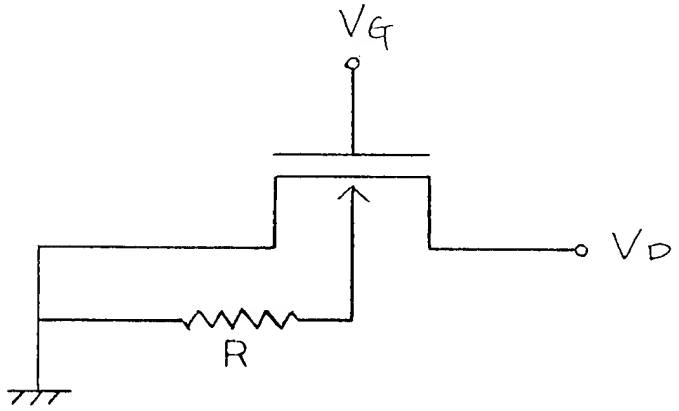


FIG. 26

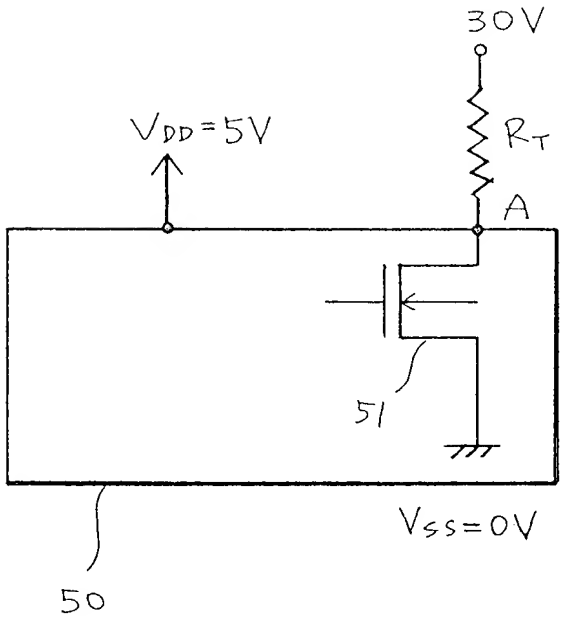


FIG. 27A

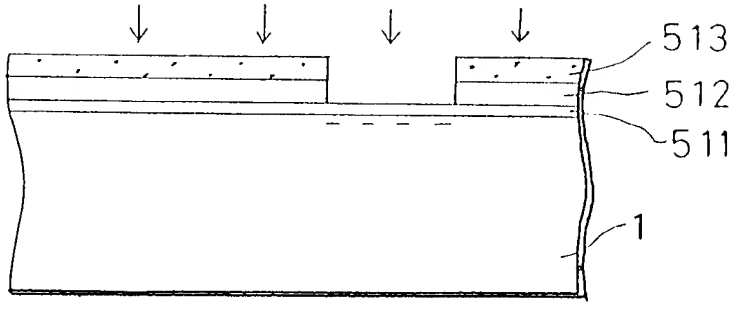


FIG. 27B

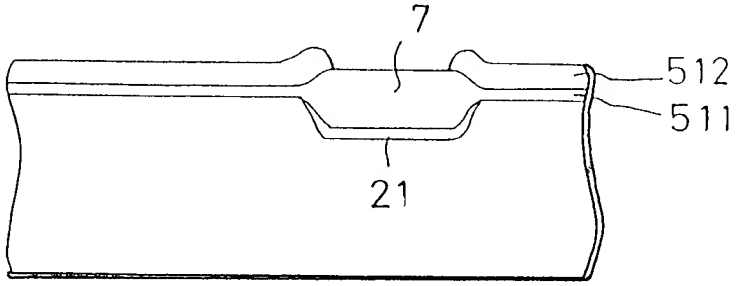


FIG. 27C

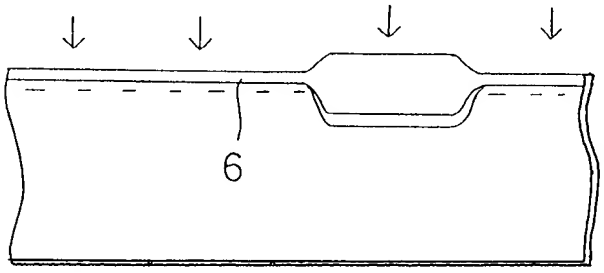


FIG. 27D

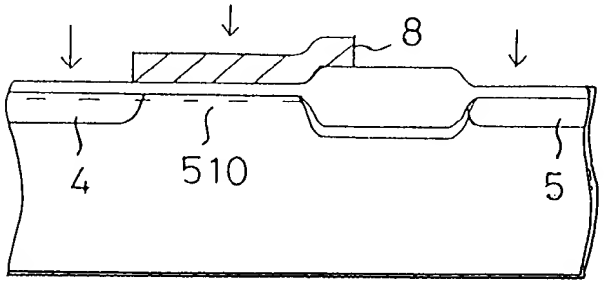


FIG. 28

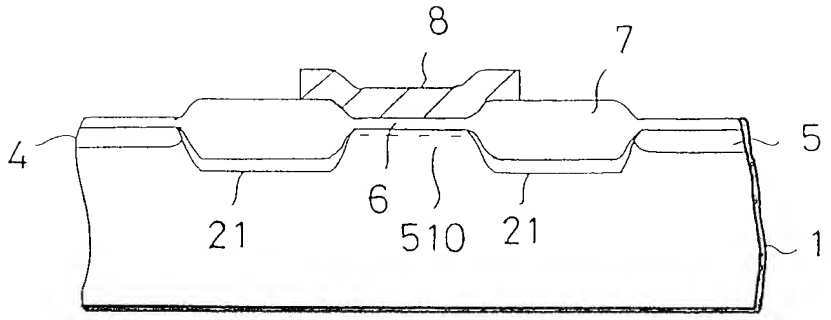


FIG. 29

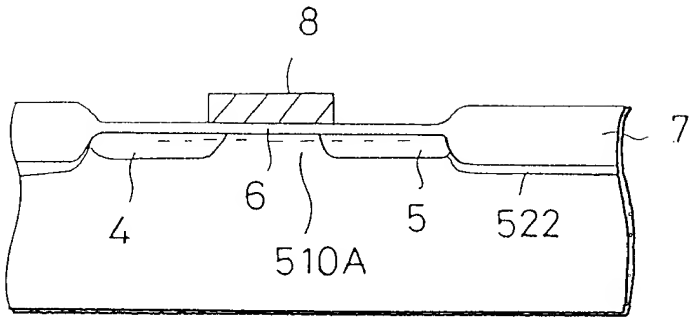
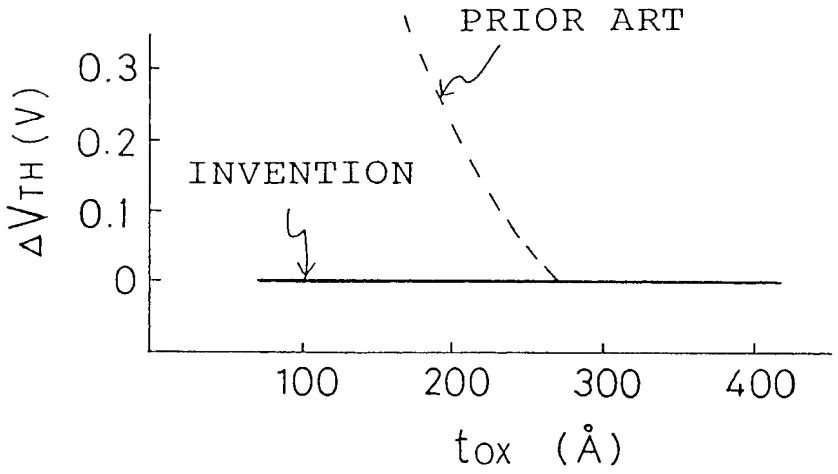


FIG. 30



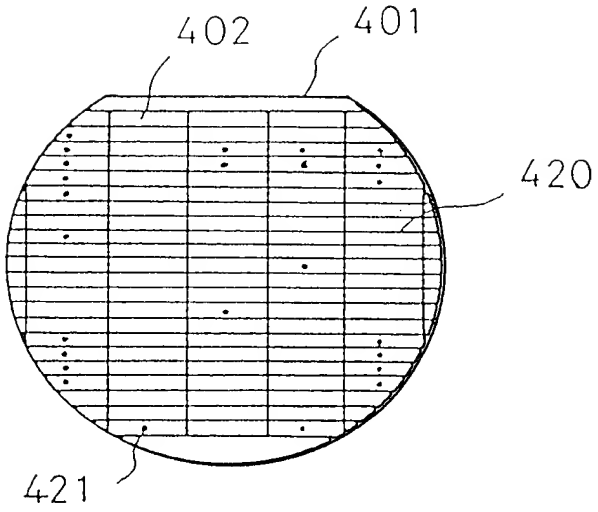


FIG. 31A

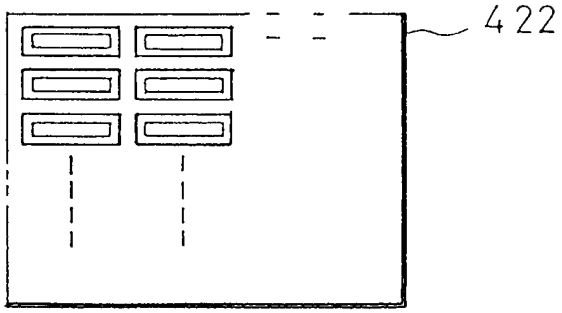


FIG. 31B

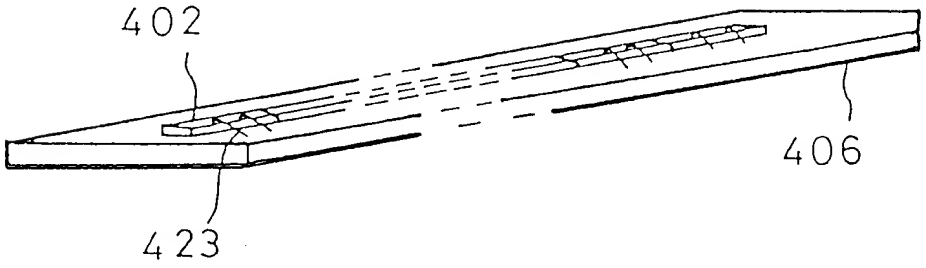


FIG. 31C

FIG. 32

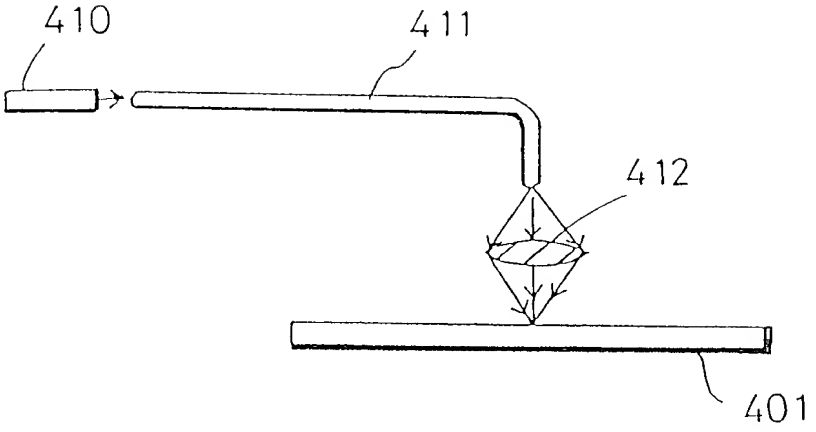


FIG. 33

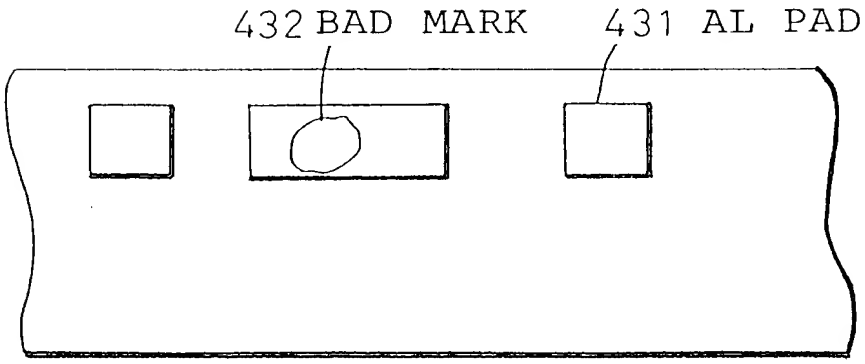


FIG. 34

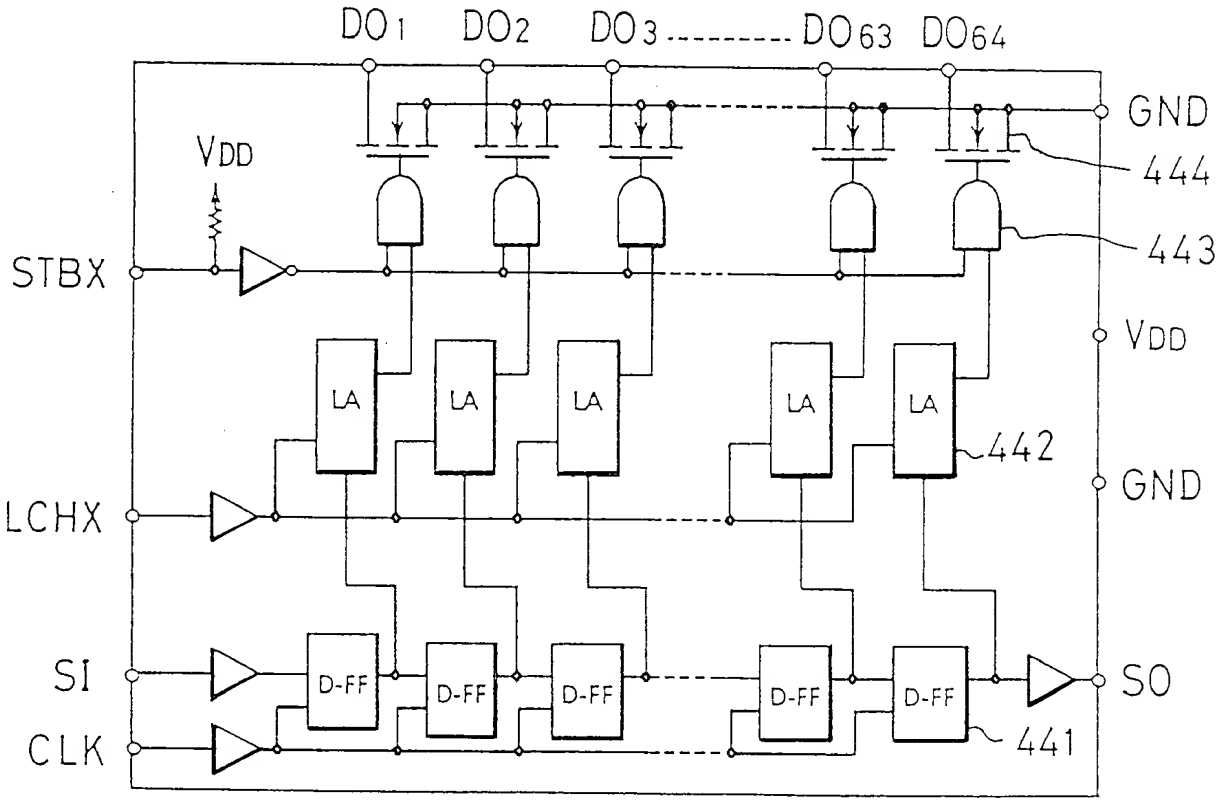

DO1
DO2
DO3
DO63
DO64
GND
444
443
VDD
STBX
LA
442
LCHX
GND
SI
D-FF
SO
CLK
441

FIG. 35

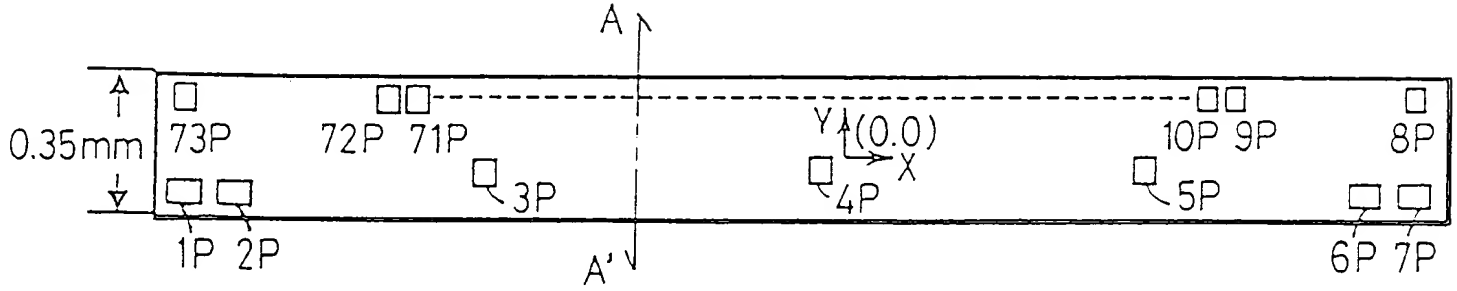


FIG. 36

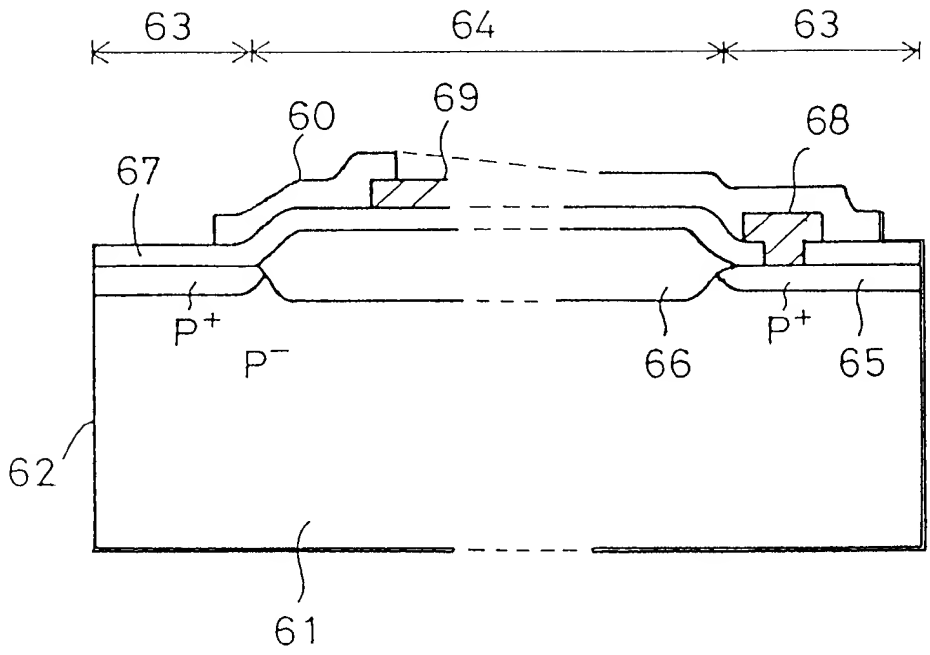


FIG. 37

Pad No.	Pad Name	Function
1P	CLK	Clock input terminal of 64-bit shift register
2P	LCHK	Data latch signal input terminal LCHX = "L" : Read shift register data LCHX = "H" : Latch immediately preceding data
3P,4P,5P	GND	GND terminals (0V)
6P	VDD	Logical circuitry positive power supply terminal (+5V)
7P	STBX	Driver strobe input terminal. Latched data output to driver at "L" input (Internal pullup resistance R_P=300KΩ TYP.)
8P	SO	64-bit shift register serial data output terminal
9P-72P	DO1-DO64	Driver output terminal (Nch open drain output)
73P	SI	64-bit shift register serial data input terminal